

Information Disclosure Statement
January 15, 2002
Page 3

#2
EL896635543US

J107 U.S. PRO
10/05/15
01/15/02

Form PTO-1449 (Modified)	ATTY DOCKET NO. B-3752DIV 619413-2	U.S. SERIAL NO. Not yet assigned
LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANT Daniel Yap, et al.	
	FILING DATE concurrently herewith	GROUP unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUB-CLASS	FILING DATE OR 102(e) DATE IF APPROPRIATE
LT	3,663,184	5/1972	Wood, et al.			
	4,661,375	4/1987	Thomas			
	5,492,235	2/1996	Crafts, et al.			
	5,763,456	4/1998	Akram			
	5,767,010	6/1998	Mis, et al.			
	5,773,359	6/1998	Mitchell, et al.			
	6,133,136	10/2000	Edelstien			
	5,162,257	11/1992	Yung			9/1991
	5,376,584	12/1994	Agarwala			12/1992
	5,480,835	1/1996	Carney, et al.			12/1994
LT	5,767,010	6/1998	Mis, et al.			11/1996

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO
LT	JP-61225839-A	10/1986	JPO			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

LT	Imler, W.R., "Precision Flip-Chip Solder Bump Interconnects for Optical Packaging," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 15, no. 6 (Dec. 1992), Pp. 977-981.
LT	Kawanobe, T., et al., "Solder Bump Fabrication by Electrochemical Method for Flip Chip Interconnection," IEEE, Publication CH1671-7/0000 (1981), pp. 149-155.
LT	Yung, E.K., et al. "Flip-chip Process Utilizing Electroplated Solder Joints," MCNC Technical Report TR90-43, October 1990.

EXAMINER	DATE CONSIDERED
(B LUAN THAI)	3/03

REMARKS: Initial if reference considered, whether or not citation is in conformance with 35 USC 102; Draw line through citation if not in conformance and NOT considered. Include copy of this form with next communication to applicant.